Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **N. CLEAR**
2. **1Q**
3. **1D**
4. **2D**
5. **2Q**
6. **3Q**
7. **3D**
8. **4D**
9. **4Q**
10. **GND**
11. **CLK**
12. **5Q**
13. **5D**
14. **6D**
15. **6Q**
16. **7Q**
17. **7D**
18. **8D**
19. **8Q**
20. **VCC**

**83 mils**

**58 mils**

**HC273G**

**MASK**

**REF**

**1 20 19**

**18**

**17**

**16**

**15**

**14**

**13**

**10 11 12**

**2**

**3**

**4**

**5**

**6**

**7**

**8**

**9**

**Top Material: Al**

**Backside Material: SiNi**

**Bond Pad Size: .0036” X .0036”**

**Backside Potential: Vcc (or floating)**

**Mask Ref: HC273G**

**APPROVED BY: DK DIE SIZE .058” X .083” DATE: 11/15/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .025” P/N: 54HC273**

**DG 10.1.2**

#### Rev B, 7/19/02